

Application No.: 10/830,107

AMENDMENT TO SPECIFICATION

Please amend the paragraph beginning on page 11, line 15 as follows:

—Next, the analog signal having a constant amplitude due to the VGA 11 is received by the analog low-pass filter (LPF) 12. The analog LPF 12 reduces noise which may be a factor for inhibiting processing in a signal processing section in the subsequent stage and is located in the outside of a signal band and, at the same time, t, a high frequency component of the input analog signal is removed [[o]] to prevent a folding strain generated in the A/D converter 14.--

Please amend the paragraph beginning on page 9, line 11 as follows:

—As shown in FIG. 1, the optical disc device of this embodiment includes a variable gain amplifier (VGA) 11 for dynamically amplifying a weak signal output from an optical pickup 100 to a predetermined amplitude level; an analog low-pass filter 12 for removing a high frequency noise component from the analog signal amplified to the predetermined amplitude level; an offset control circuit 13 for adjusting a shift (offset) from the center axis of an amplitude of the analog signal so that the analog signal is located within a dynamic range of an A/D converter 14 in the subsequent stage; the A/D converter 14 for performing oversampling to an analog signal A1 which has been offset-adjusted at a frequency n times higher than that of a channel clock (where n is 2 or a larger integer, and this condition will be used hereafter) to convert the analog signal A1 into a first digital signal D1 and outputting the first digital signal; a digital equalizer 15 for digitally performing a wave-form equalization of the reproduction signal which has been converted into the first digital signal D1 and outputting a second digital signal D2; an amplitude information detection circuit 16 for detecting amplitude information from the first digital signal D1, generating control information for the VGA 11 from the detected amplitude information, and outputting the control information to the VGA 11; an offset detection circuit 17 for detecting an

Application No.: 10/830,107

offset amount of the first digital signal **D1** to control the offset control circuit **13**; a PLL (phase-locked loop) circuit **18** as a clock extraction circuit for extracting a synchronous system clock signal for A/D conversion from the second digital signal **D2** and outputting the extracted system clock signal to the A/D converter **14** and the digital equalizer **15**; a frequency divider **19** for dividing a frequency of the second digital signal **D2** generated by the PLL circuit **18** to obtain a channel clock; a downsampling circuit **20** for performing so-called "downsampling" for changing the frequency of the oversampled second digital signal **D2** back to a frequency (i.e., channel rate) for defining a channel clock; an adaptive filter for compensating, using as an input signal a signal output from, for example, the downsampling circuit **20** which improves reliability of the second digital signal **D2**, a strain of the input signal, or an operational circuit **21** for performing Viterbi decoding using PRML (partial response maximum likelihood); and a binarizer circuit **22** for binarizing the input analog signal which is to be output from this device.--